CLAIMS

What is claimed is:

1. A power-on reset circuit comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices of one V_t for determining a power reset trigger level; and

a voltage divider connected to an input of the Schmitt-trigger circuit and configured to track a supply signal.

2. The power-on reset circuit according to claim 1, and further comprising a compensate circuit for generating a small reset pulse to compensate for temperature and a supply signal variation effect.

3. The power-on reset circuit according to claim 1, wherein the voltage divider includes a current source transistor operative to generate a current in response to a supply signal.

4. The power-on reset circuit according to claim 1, wherein the voltage divider includes a large low-side resistor for reduction of leakage current.

5. The power-on reset circuit according to claim 1, wherein the voltage divider includes a compensate circuit operative to adjust a feedback current to restore a voltage at the input of the Schmitt-trigger circuit, in response to a fluctuation in the supply signal.

6. The power-on reset circuit according to claim 1, wherein the Schmitt trigger circuit further comprises a threshold-enhancement node having a first voltage greater than zero when the Schmitt trigger circuit enters and exits a power-down mode and having a second voltage less than the first voltage when the Schmitt trigger enters and exits a sleep mode.

7. The power-on reset circuit according to claim 1, wherein the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first voltage in response to an increase of a supply signal when the supply signal has compared favorably to a first threshold voltage, and to drop from the first voltage to the ground potential when the supply signal has not compared favorably to the first threshold voltage, if the Schmitt trigger circuit has not entered a sleep mode.

8. The power-on reset circuit according to claim 1, wherein the Schmitt trigger circuit further comprises a reset signal node having a first voltage peak when the Schmitt trigger circuit enters a power-down mode and having a second voltage peak, which is greater than the first voltage peak, when the Schmitt trigger circuit exits a power-down mode..

9. The power-on reset circuit according to claim 8, wherein the reset signal node further has a third voltage when the Schmitt trigger circuit enters and exits a sleep mode and wherein the third voltage is less than the first voltage peak.

10. A method for providing a reset signal in response to a supply signal, the method comprising:

generating a primary current in response to the supply signal;

generating a trigger voltage in response to the primary current;

if a sleep mode has not been entered and the supply signal has not compared favorably to a first threshold level, increasing a reset signal from a reference potential to a first potential in response to an increase in the supply signal; and

if a sleep mode has not been entered and the supply signal has compared favorably to a first threshold level, setting the reset signal to the reference potential.

11. The method for providing a reset signal in response to a supply signal of claim 10, wherein:

the reset signal is increased from a reference potential to a first potential in response to an increase in the supply signal when a power-up state is entered;

the reset signal is increased from a reference potential to a second potential in response to an decrease in the supply signal when a power-down state is entered; and

the first potential is greater than the second potential.

12. The method for providing a reset signal in response to a supply signal of claim 11, further comprising compensating the trigger voltage in response to a change in temperature, wherein the compensating of the trigger voltage in response to a change in temperature includes:

providing a primary current path having a current corresponding to the trigger voltage; and

in a circuit having a complementary temperature coefficient with respect to a current source, adjusting the current of the primary current path to compensate the current for temperature-dependent current variations.

13. The method for providing a reset signal in response to a supply signal of claim 12, wherein the adjusting of the current of the primary current path to compensate the current for temperature-dependent current variations includes:

providing a compensation path in parallel to a low-end portion of the current path; and

increasing a compensation current in the compensation path in response to a decrease in the primary current, and decreasing a compensation current in the compensation path in response to an increase in the primary current.

14. A computer system comprising:

a microprocessor;

a bus coupled to the microprocessor;

a memory coupled to the bus; and

a power-on reset circuit operative to generate a power-on reset signal to the microprocessor, the power-on reset circuit comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices of one V_t for determining a power reset trigger level; and

a voltage divider connected to an input of the Schmitt-trigger circuit for tracking a supply signal..

15. The computer system of claim 14, wherein the power-on reset circuit further comprises a compensate circuit for generating a small reset pulse to compensate for temperature and a supply signal variation effect.

16. The computer system of claim 14, wherein the voltage divider includes a current source transistor operative to generate a current in response to a supply signal.

17. The computer system of claim 14, wherein the voltage divider includes a large low-side resistor for reduction of leakage current.

18. The computer system of claim 14, wherein the voltage divider includes a compensate circuit operative to adjust a feedback current to restore a voltage at the input of the Schmitt-trigger circuit, in response to a fluctuation in temperature.

19. The computer system of claim 14, wherein the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first voltage in response to an increase of a supply signal when the supply signal has compared favorably to a first threshold voltage, and to drop from the first voltage to the ground potential when the supply signal has not compared favorably to the first threshold voltage, if the Schmitt trigger circuit has not entered a sleep mode.

20. The computer system of claim 14, wherein the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first voltage in response to a change of a supply signal during either a power-up or power-down mode but not during an entering or exiting of a sleep mode.

21. The computer system of claim 20, wherein:

the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first voltage in response to a change of a supply signal during a power-up mode and to rise from a ground potential to a second voltage in response to a change of the supply signal during a power-down mode; and

the first voltage is greater than the second voltage.

22. The computer system of claim 14, wherein:

the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first voltage in response to a change of a supply signal during a power-up mode and to rise from a ground potential to a second voltage in response to a change of the supply signal during a power-down mode; and

the first voltage is greater than the second voltage.